REMARKS

Reconsideration of the application in view of the following remarks is respectfully requested.

The Examiner rejects claims 1-14 and 16-20 under 35 U.S.C. § 102(e) as being anticipated by Kelly et al. The Examiner states that Kelly discloses a PCI Express to PCI bridge as shown in FIGURE 9 and a port arbitration circuit as shown in FIGURE 8. The Examiner states that a PCI Express interface, as a serial interface coupled between the virtual channel arbitration circuit and the output port is shown in FIGURE 9.

This rejection is respectfully traversed. Kelly et al. shows both a PCI Express switch and a PCI to PCI Express bridge. FIGURE 9 illustrates the PCI to PCI Express bridge, as clearly recited in the Brief Description of the Drawings. However, FIGURE 8 illustrates a PCI Express switch, which is a completely different device. As known to those skilled in the art, a PCI Express switch is specifically provided for in the PCI Express specification and is a serial in to serial out device because PCI Express is a switched fabric whereas PCI is a parallel bus. Accordingly, those skilled in the art know that a PCI Express switch as shown as FIGURE 8 can not be used with a PCI bus. The circuit shown in FIGURE 9, which is a completely different circuit, can be connected to a PCI bus and provides a serial I/O interconnect to a PCI Express fabric. It is therefore a bridge between these two standards.

Accordingly, when the Examiner states that the PCI Express to PCI bridge of FIGURE 9 comprises portions shown in FIGURE 8, this is clearly incorrect. These are separate devices and not portions of a single device. It should be noted that the inputs and outputs of the device in FIGURE 8 go through serial interfaces and SERDES (serializer/deserializer) which is incompatible with a parallel bus connection.

Furthermore, the present invention controls the grant and stop lines of the PCI compatible devices in order to use a time based port arbitration table from PCI Express to enforce a time based arbitration on the PCI devices, whereas PCI does not support this feature. When all devices are connected to a parallel bus, such as the PCI bus, the

bridge, such as bridge 112 shown as FIGURE 1, each of the devices has equal priority which may interfere with the sending of isochronous data because there is no way to prioritize between data that can wait and data that has no value if it does not arrive on time. Thus, the present invention overcomes the limitation of the prior art bus design to allow such devices to be utilized in a PCI Express fabric which does support the transmission of isochronous data without the cost of replacement of these devices. Claims 1 and 16 have been amended in this respect.

With regard to claims 19 and 20, the Examiner refers to Kelly at Col 7, LL 17 – Col 8, LL 67 and talks about receiving data from a PCI compatible device, which is clearly contrary to the text of Kelly, et al. For example, LL 15-17 of Col 7 recites "In the simplest case for an Express switch, only one input buffer set and only one output buffer set are required..." (Emphasis added). Thus, the description in FIGURE 7 and 8 is for a PCI Express switch, which, as described above, can not be coupled to a PCI bus. Accordingly, those claims have only been changed to change the term PCI Express or PCI Express fabric, as discussed below.

The Examiner rejects claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Kelly et al. in view of Hewitt et al. The Examiner states that Kelly et al. discloses all of limitations above except for these of an IEEE 1394 device. The Examiner states that Hewitt discloses a I/O module that can include an IEEE 1394 link. Claim 15 is indirectly dependent of Claim 1. The patentability of Claim 1 having been shown above, Claim 15 is patentable for the same reasons.

In the prosecution of another application concerning PCI Express, Applicant has been informed that the term PCI Express has been trademarked and is therefore inappropriate in a patent claim. Accordingly, the claims have been amended in order to eliminate the terms PCI Express or PCI Express fabric and replace them with a description thereof in order avoid this problem, although it was not raised by the Examiner in this Application.

Accordingly, Applicants believe the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
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